REMARKS

Claim 57 is amended. New claims 75-79 are added. Claims 42-79 are pending in the application for consideration.

Claim 42 stands rejected under 35 U.S.C. §102(e) as being anticipated by Jiang et al. (U.S. Patent No. 6,048,755). Claim 57 stands rejected under 35 U.S.C. §102(b) as being anticipated by Nakashima et al. (U.S. Patent No. 5,661,086). Claims 43-45, 49, 50 and 55-56 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Chen et al. (U.S. Patent No. 6,215,180). Claims 46 and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Chen and further in view of Tummala et al., Packaging Handbook-Semiconductor Packaging, Part II, 2nd Edition, 1997, pgs. 898-901. Claim 48 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Chen and further in view of Tummala et al, Packaging Handbook-Semiconductor Packaging, Part III, 2nd Edition, 1997, pp. 223-234. Claims 51-54 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Chen and further in view of Wang et al. (U.S. Patent No. 6,255,140). Claims 63-67 stand rejected under the judicially created doctrine of obviousness-type double patenting.

Claims 58-62 stand objected to as being dependent upon a rejected base claim. Claims 68-74 are allowed.

Regarding the anticipation rejection against claim 42 based on Jiang, claim 42 recites adhering a semiconductive-material-comprising die to a substrate with an electrically conductive adhesive. Jiang fails to teach such limitation of claim

42. Jiang teaches a die 16 is bonded directly to a substrate 56 using adhesive layer 72 which can comprise a filled epoxy, an unfilled epoxy, an acrylic, or a polyamide material (col. 6, lines 8-15). In no reasonable or fair interpretation does such a teaching of Jiang suggest or disclose adhering a semiconductive-material-comprising die to the substrate with an **electrically conductive** adhesive as recited in claim 42. Accordingly, Jiang fails to teach a positively recited limitation of claim 42, and therefore, the anticipation rejection fails and should be withdrawn. Applicant respectfully requests allowance of claim 42 in the next office action.

Claims 43-44 depend from independent claim 42, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Moreoever, claims 43-44 stand rejected over Jiang in view of Chen. Such combination of art is improper under Section 35 U.S.C. §103(c), and therefore, the rejection is inappropriate and should be withdrawn. Jiang, U.S. Patent No. 6,048,755, and the above-referenced application, are commonly owned. The Examiner is respectfully reminded that Section 35 U.S.C. §103(c), addressed at MPEP §706.02(l)(3) (8th Edition), states that such commonly owned reference is disqualified when: (A) proper evidence is filed [referring to the statement of common ownership]; (B) the reference qualifies under 35 U.S.C. §102(e) for applications filed on or after November 29, 1999; and (C) the references used in an obviousness rejection under 35 U.S.C. §103(a).

Regarding (A), a separate statement establishing common ownership is filed herewith. Regarding (B), the Jiang reference qualifies under §102(e), and the above-referenced application was filed on January 9, 2001. Regarding (C), the above-referenced claims are rejected in an obviousness rejection under Jiang as a primary reference. Accordingly, the requirements of MPEP §706.02 and §103(c) are met, and therefore, the obviousness rejections based on Jiang are inappropriate and should be withdrawn. Claims 43-44 are allowable for this additional reason and Applicant respectfully requests allowance of claims 43-44 in the next office action.

Claims 44-56 stand rejected over various combinations of art with Jiang as the primary reference. For the reasons discussed above with respect to dependent claims 43-44, Jiang is an improper reference for an obviousness rejection since the reference and above-referenced application are commonly owned. Consequently, the obviousness rejections against claims 45-56 fail and should be withdrawn. Claims 45-56 are allowable and Applicant respectfully requests allowance of claims 45-56 in the next office action.

Regarding the anticipation rejection against claim 57 based on Nakashima, claim 57 is amended to recite adhering a semiconductive-material-comprising die to a metal foil and substrate. No new matter is added as the originally-filed application supports the amended language at, for example, page 10 and Fig. 6. Nakashima does not teach such limitation of claim 57. Nakashima teaches adhering a semiconductor die 14 to a metal substrate 12 **only** (col. 6, lines 5-9; Figs. 1 and 4). In no fair or reasonable interpretation does Nakashima teach

or suggest adhering a semiconductive-material-comprising die to the metal foil **and** substrate as recited in claim 57. Accordingly, Nakashima fails to teach a positively recited limitation of claim 57, and therefore, claim 57 is allowable. Applicant respectfully requests allowance of claim 57 in the next office action.

Claims 58-62 depend from independent claim 57, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Claims 63-67 stand rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-11 of U.S. Patent Nos. 6,214,641, 5,998,865, 5,817,535 and 5,723,907. Such a rejection is inappropriate as U.S. Patent No. 5,817,535 is a divisional patent from U.S. Patent No. 5,723,907. During the prosecution of U.S. Patent No. 5,723,907, the Examiner presented a restriction requirement in an office action mailed 12-2-96 (paper no. 2) between claims drawn to a semiconductor device and claims drawn to a method of making semiconductor devices wherein the Examiner stated the inventions of such claims **are distinct**. Applicant elected to prosecute the claims drawn to the semiconductor device in U.S. Patent No. 5,723,907 and the claims drawn to the method of making semiconductor devices were prosecuted in U.S. Patent No. 5,817,535. Consequently, the obviousness-type double patenting rejection over all four patents is inappropriate and should be withdrawn. Applicant respectfully requests a clarification of this rejection in a subsequent non-final office action.

New claims 75-79 are rewritten claims 58-62, respectively, which stood objected to for depending from a rejected base claim. Consequently, new claims 75-79 are allowable.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed together with this application on April 1, 2002. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 7-30-02

By: _____

D. Brent Kenady
Reg. No. 40,045

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/756,971
Filing Date . . . . . January 9, 2001
Inventor . . . . . Salman Akram
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2827
Examiner . . . . . David A. Zarneke
Attorney's Docket No. MI22-1572
Title: Methods of Forming Board-On-Chip Packages

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 30, 2002 DATE OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

57. (Amended) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil and substrate, the die having circuitry supported thereby; and

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening.